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**Assignment 2**

1. Consider a 130 nm technology. Compute the value of *VDSAT* for the NMOS and PMOS device assuming *VGS* = 1.2 V, *VTn* = 0.4 V, *VTp* = -0.4 V, *L* = 100 nm.
2. Compute the NMOS and PMOS saturation currents per micron of width for a 180 nm technology and the ratio of IDSATN/IDSATP. Assume a channel length of 200 nm, *tox* = 35 Å, *VTn*= 0.5 V, *VTp* = -0.5 V, *VGS* = 1.8 V. Use *νsat* = 8\*106 cm/s.
3. Compute the channel capacitance in the cutoff, resistive, and saturation regions required for a NMOS device with *tox* = 22 Å and *W* = 400 nm, *L* = 100 nm.
4. Compute the junction capacitance for a 130 nm technology.

(a) Find *Φ0* and *Cjo* for an n+p junction with *ND* = 1020 cm-3 and *NA* = 3\*1017 cm-3.

(b) *W* = 400 nm, *L* = 100 nm, *xj* = 50 nm, and the diffusion extension *LS* is 300 nm. Find *Cdiff* in unit of fF for *VD* = 0 V and *VD* = -1.2 V. Assume *Cj* = *C’jsw*.

1. Using HSPICE and TSMC 0.18 µm CMOS technology model with 1.8 V power supply, plot the sub-threshold current *IDSUB* versus *VBS*, and the saturation current *IDSAT* versus *VBS*for an NMOS device with *W* = 400 nm and *L* = 200 nm. Specify the range for *VBS* as 0 to –2.0 V. Explain the results.
2. Using HSPICE and TSMC 0.18 um CMOS technology model with 1.8 V power supply, plot log *IDS* versus *VGS* while varying *VDS* for an NMOS device with *L* = 200 nm, *W* = 800 nm and a PMOS with *L* = 200 nm, *W* = 2 µm. Explain the results.

**Answer:**

1. Consider a 130 nm technology. Compute the value of *VDSAT* for the NMOS and PMOS device assuming *VGS* = 1.2 V, *VTn* = 0.4 V, *VTp* = -0.4 V, *L* = 100 nm.

VDSAT=K(VGT)VGT|(VGT=VGS-VT)=(VGS-VT)/(1+(VGS-VT)/ξcL)

ξcnLn=6\*104\*0.1\*10-4=0.6V

ξcpLp=24\*104\*0.1\*10-4=2.4V

NMOS:VDSAT=(1.2-0.4)/(1+(1.2-0.4)/0.6)=0.343V

PMOS:VDSAT=(1.2-0.4)/(1+(1.2-0.4)/2.4)=0.6V

1. Compute the NMOS and PMOS saturation currents per micron of width for a 180 nm technology and the ratio of IDSATN/IDSATP. Assume a channel length of 200 nm, *tox* = 35 Å, *VTn*= 0.5 V, *VTp* = -0.5 V, *VGS* = 1.8 V. Use *νsat* = 8\*106 cm/s.

IDAST=vsatCOX(VGS-VT-VDSAT)W=vsatCOXW(VGT2/(VGT+ξcL))

ξcnLn=6\*104\*0.2\*10-4=1.2V

ξcpLp=24\*104\*0.2\*10-4=4.8V

NMOS:IDASTN/WN=8\*106\*(3.97\*8.85\*10-14/(35\*10-8))\*(1.8-0.5)2/(1.8-0.5+1.2)=8.653A/cm=541μA/μm

PMOS:IDASTP/WP=8\*106\*(3.97\*8.85\*10-14/(35\*10-8))\*(1.8-0.5)2/(1.8-0.5+4.8)=3.546A/cm=222μA/μm

IDASTN/IDASTP=2.44WN/WP

1. Compute the channel capacitance in the cutoff, resistive, and saturation regions required for a NMOS device with *tox* = 22 Å and *W* = 400 nm, *L* = 100 nm.

**cutoff:**

CGCB=COXWL=1.6\*10-6\*400\*10-7\*100\*10-7=0.64fF

CGCS=CGCD=0

**resistive:**

CGCB=0

CGCS=CGCD=1/2\*COXWL=0.32fF

**saturation:**

CGCB=CGCD=0

CGCS=2/3\*COXWL=0.427fF

1. Compute the junction capacitance for a 130 nm technology.

(a) Find *Φ0* and *Cjo* for an n+p junction with *ND* = 1020 cm-3 and *NA* = 3\*1017 cm-3.

Φ0=Φ1ln(NAND/ni2)=26\*ln(1020\*3\*1017/(2.25\*1020))=1.025V

Cjo*=*=(11.7\*8.85\*10-14\*1.6\*10-19\*0.5\*1020\*3\*1017/(1020+3\*1017)/1.025)0.5=1.555\*10-7F/cm2=1.555fF/μm2

(b) *W* = 400 nm, *L* = 100 nm, *xj* = 50 nm, and the diffusion extension *LS* is 300 nm. Find *Cdiff* in unit of fF for *VD* = 0 V and *VD* = -1.2 V. Assume *Cj* = *C’jsw*.

Cj=Cj0/(1-VD/Φ0)0.5

**VD = 0 V:**

Cj=Cj0=1.555fF/μm2

Cbottom=CjWLS+Cj(W+2LS)xj=1.555\*(0.4\*0.3+(0.4+0.6)\*0.05)=0.264fF

**VD = -1.2 V:**

Cj=Cj0/(1-VD/Φ0)0.5=1.555/(1+1.2/1.025)0.5=1.055fF/μm2

Cbottom=CjWLS+Cj(W+2LS)xj=1.055\*(0.4\*0.3+(0.4+0.6)\*0.05)=0.179fF

1. Using HSPICE and TSMC 0.18 µm CMOS technology model with 1.8 V power supply, plot the sub-threshold current *IDSUB* versus *VBS*, and the saturation current *IDSAT* versus *VBS*for an NMOS device with *W* = 400 nm and *L* = 200 nm. Specify the range for *VBS* as 0 to –2.0 V. Explain the results.

**sub-threshold current IDSUB versus VBS：**

\* SPICE INPUT FILE: Bsim3demo1.sp IDSUB-VBS

.param Supply=1.8 \* Set value of Vdd

.lib 'D:\Synopsys\tsmc018\mm018.l' TT \* Set 0.18um library

.opt scale=0.1u \* Set lambda

.OPTION POST

mn Vdd gaten Gnd bn nch l=2 w=4 ad=20 pd=4 as=20 ps=4

Vdd Vdd 0 'Supply'

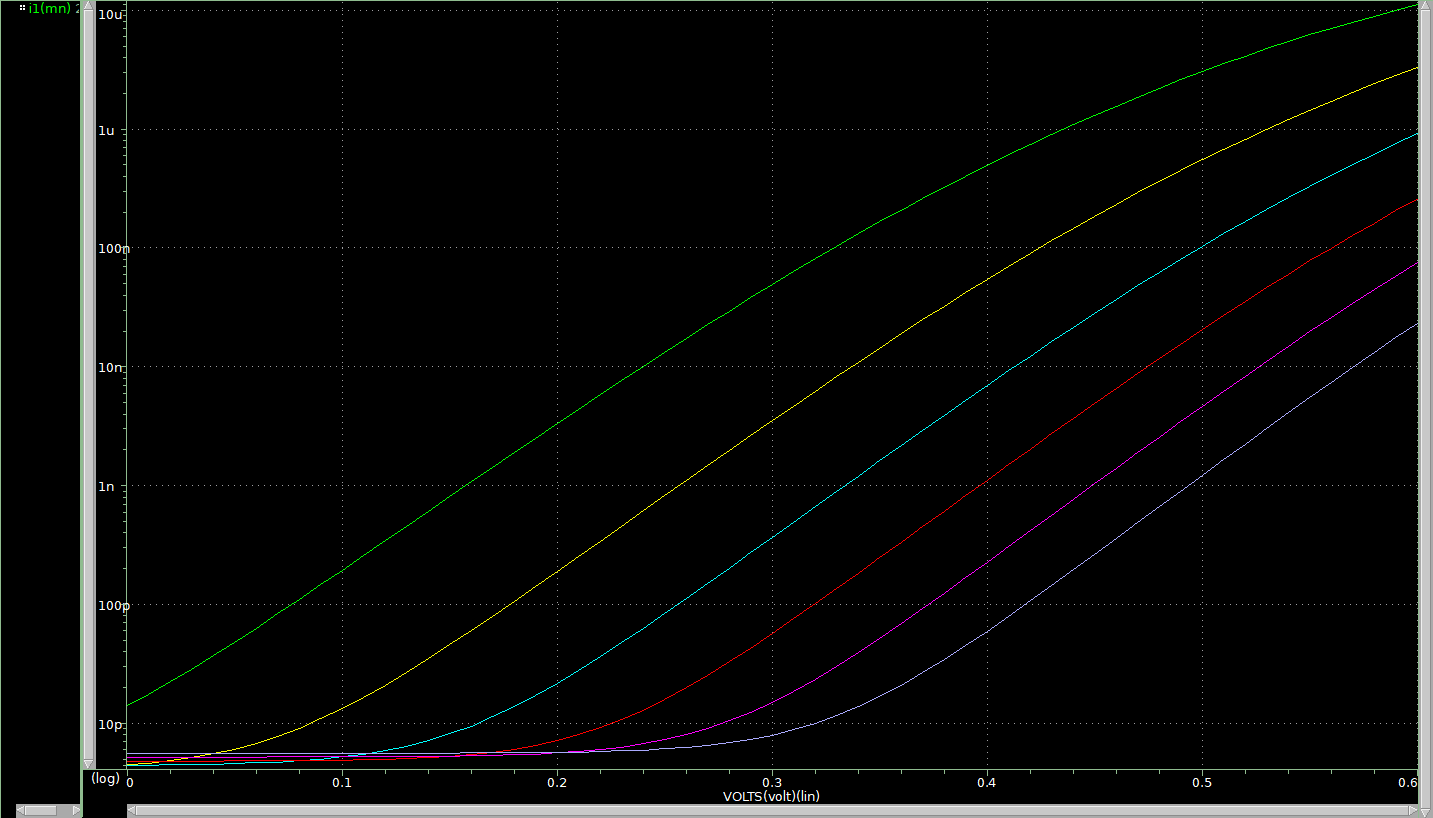
Vgsn gaten Gnd dc

Vbsn bn Gnd dc

.dc Vgsn 0 0.6 0.01 Vbsn 0 -2 -0.4

.print dc I1(mn)

.end



**saturation current IDSAT versus VBS：**

\* SPICE INPUT FILE: Bsim3demo1.sp IDSAT-VBS

.param Supply=1.8 \* Set value of Vdd

.lib 'D:\Synopsys\tsmc018\mm018.l' TT \* Set 0.18um library

.opt scale=0.1u \* Set lambda

.OPTION POST

mn Vdd gaten Gnd bn nch l=2 w=4 ad=20 pd=4 as=20 ps=4

Vdd Vdd 0 'Supply'

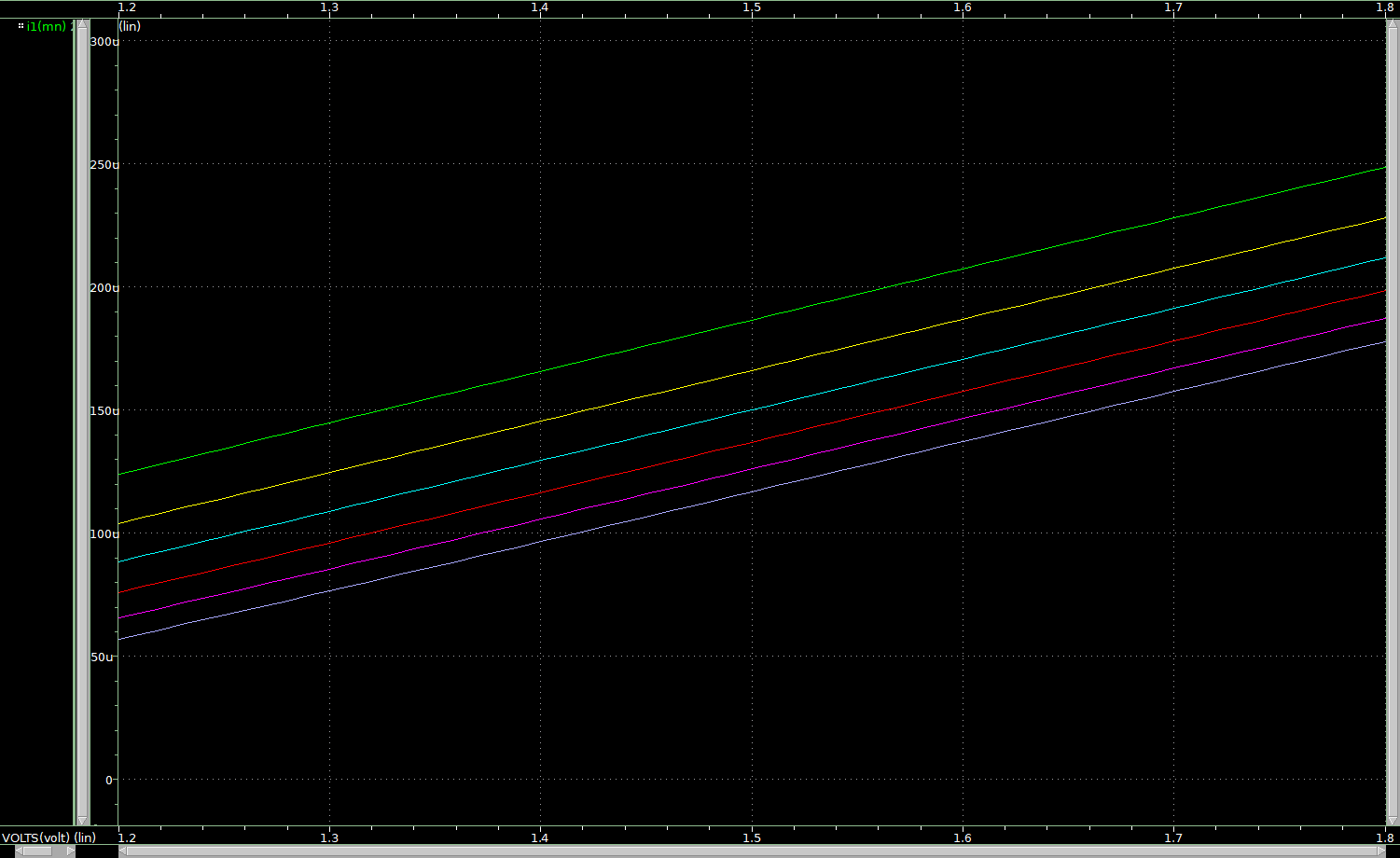
Vgsn gaten Gnd dc

Vbsn bn Gnd dc

.dc Vgsn 1.2 1.8 0.01 Vbsn 0 -2 -0.4

.print dc I1(mn)

.end



从图中可以看出，随着VBS从0变化到-2V，其会使得沟道发生强反型时的表面电势增大，阈值电压逐渐增大，亚阈值电流和饱和电流逐渐减小。

1. Using HSPICE and TSMC 0.18 um CMOS technology model with 1.8 V power supply, plot log *IDS* versus *VGS* while varying *VDS* for an NMOS device with *L* = 200 nm, *W* = 800 nm and a PMOS with *L* = 200 nm, *W* = 2 µm. Explain the results.

\* SPICE INPUT FILE: Bsim3demo1.sp ID-VDS

.param Supply=1.8 \* Set value of Vdd

.lib 'D:\Synopsys\tsmc018\mm018.l' TT \* Set 0.18um library

.opt scale=0.1u \* Set lambda

.OPTION POST

mp drainp gatep Vdd Vdd pch l=2 w=20 ad=20 pd=4 as=20 ps=4

mn drainn gaten Gnd Gnd nch l=2 w=8 ad=20 pd=4 as=20 ps=4

Vdd Vdd 0 'Supply'

Vgsp Vdd gatep dc

Vgsn gaten 0 dc

Vdsp Vdd drainp dc

Vdsn drainn 0 dc

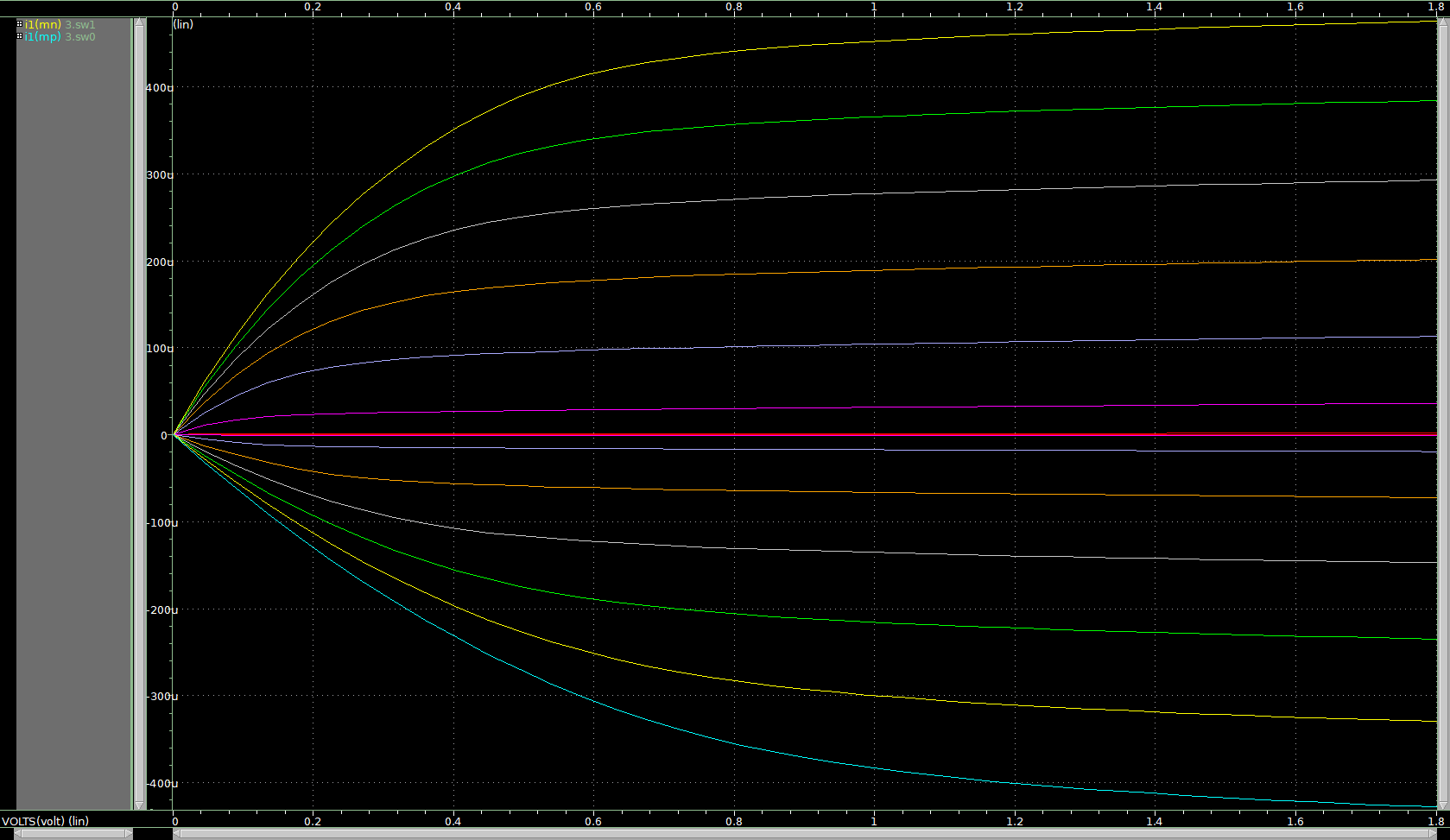
.dc Vdsp 0 'Supply' 'Supply/40' Vgsp 0 'Supply' 'Supply/8'

.dc Vdsn 0 'Supply' 'Supply/40' Vgsn 0 'Supply' 'Supply/8'

.print dc I1(mp)

.print dc I1(mn)

.end



当|VGS|<=|VTH|时，NMOS和PMOS晶体管处于截止区，IDS为0；|VGS|>=|VTH|且|VDS|<=|VGS-VTH|时，NMOS和PMOS晶体管处于线性区，IDS随VDS增加而增加；|VGS|>=|VTH|且|VDS|>=|VGS-VTH|时，NMOS和PMOS晶体管处于饱和区，沟道夹断，IDS不随VDS变化。